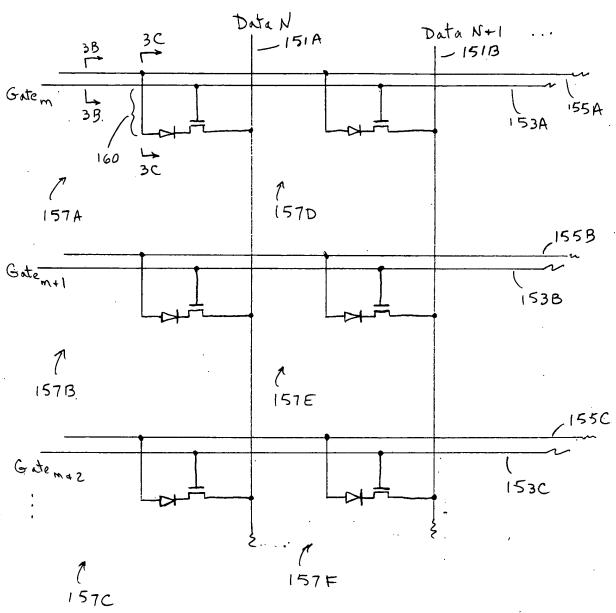
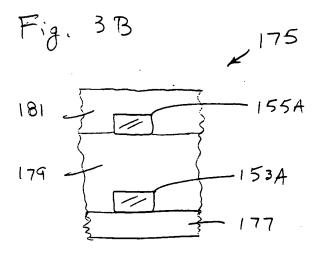


Fig. 3A 150





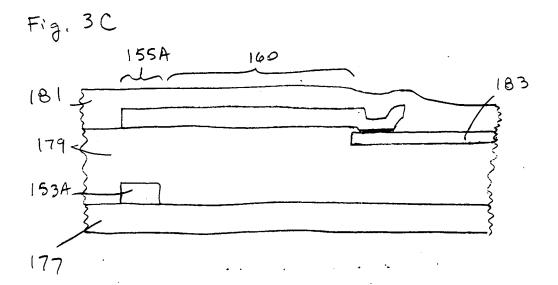
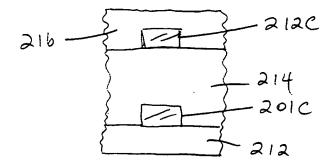
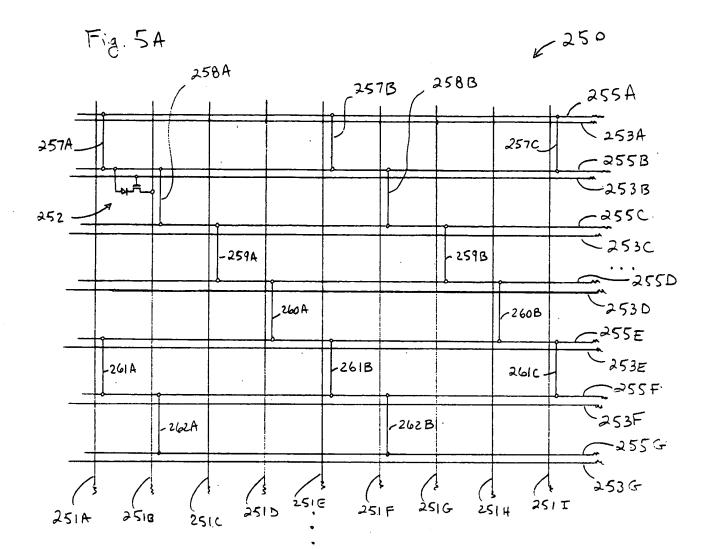
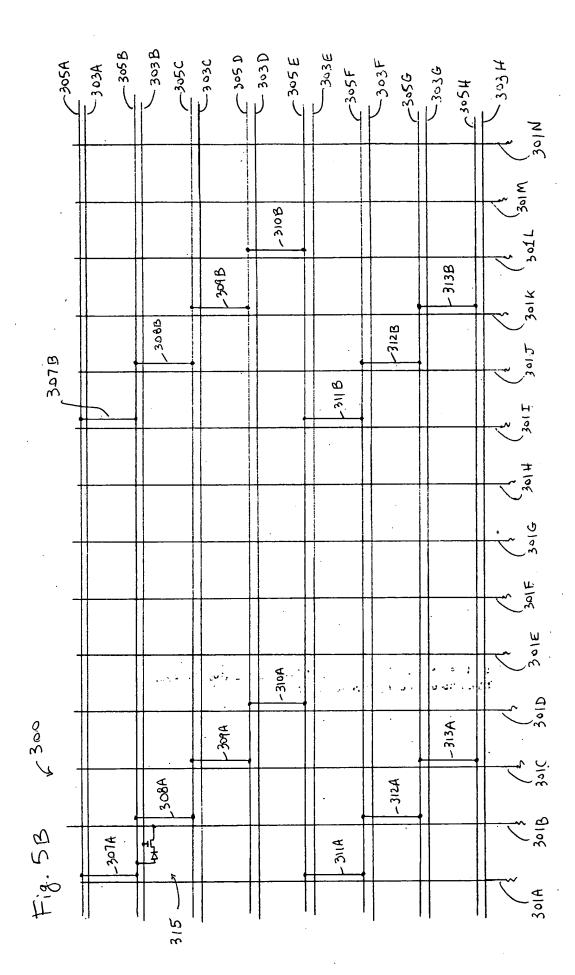


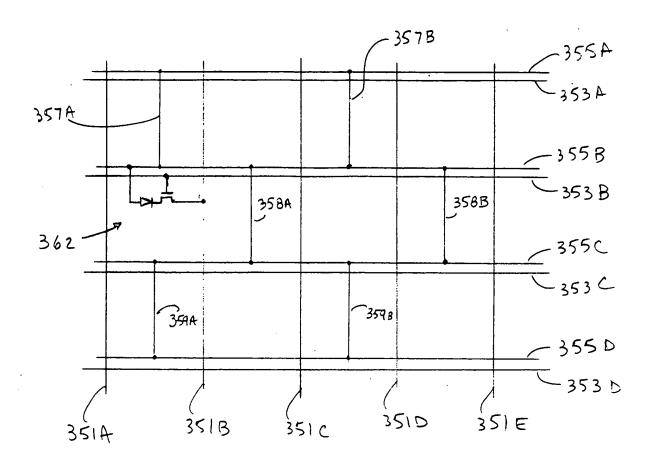
Fig. 4B



τ	Datan Da	ata D	ata D 1 n+2	ota 1 n+3	Data n+4	Data n+5
	40					2.05A
Gate 212A_	John Town					203A
20A_	77	1 2108	1210C	↑ ₂₁₀₀	210=	,205B
Gate mr1	2123-					203B
	1 210F	12106	1 210H			205C
Gate M+2		48 🖵	7,43			203C
		2120				/205D
Gate m+3			2126			203 D
			2120			205E
Gate			,			203E
				2125		205F
Gate m+5						2035
				•		
	2012	/	•		b	
	Ø 1 H	201B	201C	901D	201E	201F







and the second of the second o

The terminal of the service

Form a plurality of

gate and data lines

Form a plurality

of transistors and
photodiodes

Form a mesh of bias

voltage lines with first bias

lines parallel with gate lines

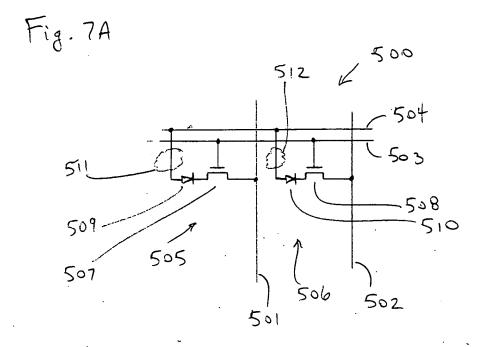
and second bias lines

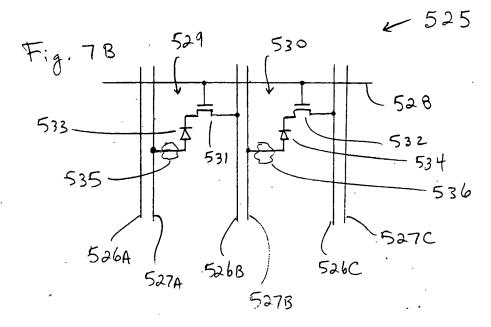
perpendicular to gate lines

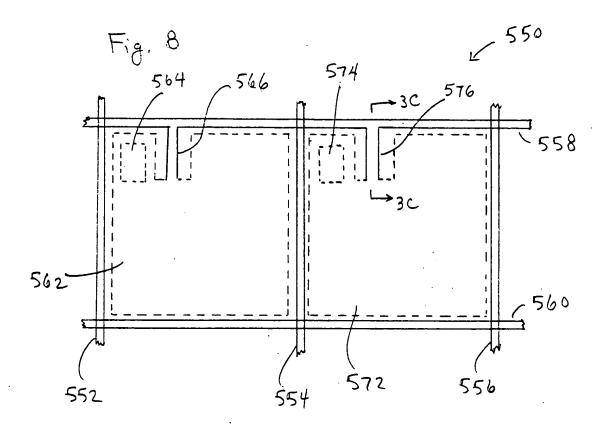
and length of first bias

lines greatly exceed length

of second bias lines







Form detecting cells with top
bias lines which include pixel
defect correcting portions which
couple bias lives to photodiodes

Test photodetector array for
defective pixels

Selectively delete defective pixels
by using pixel defect correcting
portion of defective pixel
(e.g. laser cut the bias line portion
which extends from bias line
to photodiode)